INAUGURAL ADDRESS DELIVERED BY

DR. ATMA RAM

At the Sixth Annual Conference of the Computer Society of India
at The National Aeronautical Laboratory Bangalore,
on 14th January, 1971.

Ladies and Gentlemen:

I am grateful to the authorities of the Computer Society of
India to have given me this opportunity of associating myself with
its sixth annual meeting and of expressing some of my personal views
about that novel and remarkable machine—the computer. I learn
that there are nearly two hundred delegates attending this meeting
and that more than seventy papers are to be presented. This re-
sponse is indeed heartening and speaks of the growing role the Society
is playing in helping to formulate national policies in regard to the
computer. The need for a Society of professional experts in a field
as sophisticated as Computer can hardly be over emphasised.

The laboratories of the Council of Scientific and Industrial
Research were among the first institutions to install computers in the
country. The computer in the National Aeronautical Laboratory is
one of the oldest. The installation of this computer six years ago coincided with the formation of your Society itself. It would, there-
fore, appear to be no mere accident that this Annual Meeting is
being held at the National Aeronautical Laboratory.

Computers have travelled a long way and very fast in the
last fifteen years or so, both technologically and in terms of
application. The early computers were small, not very sophisticated
and difficult to use by today's standards. May be, their impact was,
therefore, somewhat marginal. I am told that the computer had to
'programmed' in its own language which was very limited and required
long instructions and consequent possibility for errors in programming.
Only specialist programmers and operators could derive useful inform-
ation from such computers. With the passage of time these
difficulties were appreciated more and more and efforts were directed
to evolve languages more akin to human terminology. Such languages
had to be translated into the machine language, and it was soon
found that the computer itself could be made to do the translation.
Efforts to develop universal languages culminated in the development
of ALGOL, COBOL, FORTRAN and so on. The use of such languages
in computers set off an explosion of computer activity which in
turn generated the need for more and larger computers. Numerical
previously done by a number of men. A familiar example of this is the calculation of workers’ pay
bills. There can be no doubt that when a computer is proposed to be applied in such a situation,
the problem should be very carefully studied and one must not rush to use computer to accentuate
the already acute problem of educated unemployed. But more important are the applications where a
computer helps in providing opportunities for humans rather than removing them. It is not difficult
to list applications where the use of computers helps to increase the wealth of the nation, and lightens
the burden on the common man. No one will argue that the use of a computer in a flood warning
system is detrimental to the nation’s interests. Nor can one dispute that an efficient management
of the affairs of a large undertaking is in the interest of the workers themselves.

It is inconceivable for an aeronautical laboratory to function efficiently without the facilities of a
powerful computer. We must not forget that computer is a powerful tool of efficiency and precision.
It should not be considered just a calculating machine. With the ever widening network of railways,
dockyards, and airports handling traffic problems of increasing magnitude and complexity, some of
them even involving problems of delays and even possibilities of disasters, I see little possibility of
facing them successfully without the help of the big tool of big tasks. If the nation has to expand
these services, which it must for progress and prosperity, it has also to take to the computer.

I earnestly hope that nothing will be done which will obscure our vision in this vital matter and
we shall not miss the computer era but grasp it with both hands. Whatever is needed is public awareness
of computer applications so that they see their advantages as well as the disadvantages and are
enabled to make a more balanced judgement of the social impact of computers. I should appeal to
the group of professional scientists as such belonging to your Society to undertake the responsibility
and believe the results may turn out to be rewarding.

I am happy and it is appropriate that one of the CSIR laboratories, the National Aeronautical
Laboratory, under the stimulating leadership of its Director, Dr. S.R. VALLURI, is hosting the
Sixth Annual Meeting of the Computer Society. I wish the Society all success in its deliberations.

High-Speed Arithmetic on Modern Computers*
E. V. KRISHNAMURTHY
Indian Institute of Science, Bangalore-12

INTRODUCTION

Concurrently with the development of high-speed Switching devices, the theoretical Computer
arithmetic has also advanced giving rise to many strikingly novel concepts and designs to accelerate
the speed of basic arithmetic operations in the coming generation of digital computers. In this lecture
firstly we shall review some recent advances in this area and then discuss the limitations ahead.

To achieve high speeds in arithmetic the two important steps are:

1. Minimize the propagation delay through the logic nets.
2. Reorganize the basic steps which result in a given arithmetic operation - namely, devising new
   algorithms which are fast, efficient, and are compatible with the newly available hardware devices.

Our discussion here will be essentially concerned with the second step, although at the end we shall remark on the barriers which prevent us implementing step 1 to any desired degree.

It is somewhat obvious that the four basic arithmetic operations, addition, subtraction, multiplication and division are interrelated in the sense that every succeeding operation respectively is of higher complexity than the preceding one. Thus when we consider fast multiplication we are confronted with the necessity of having a fast adder and any fast division scheme has to necessarily involve high-speed addition or multiplication schemes. Therefore, it seems pertinent to review the advances, starting from the addition schemes.

**ADDITION SCHEME**

The important step in increasing the speed of addition is by decreasing the carry propagation time while carrying out a parallel addition scheme. Interesting studies have been made which give theoretical limits for the least time required to perform addition as well as multiplication; these give us the theoretical lower bounds as a function of the fan-in per stage, number of bits in operand and the delay per stage. (See Winograd (1966, 1967), Farber and Schlig (1970)). Many practical designs, particularly the carry-look-ahead and conditional-sum-adders which are very fast have been proposed. (Flores (1963), Flynn (1966)).

The principle of carry-look-ahead is to examine a number of stages of inputs to the adder and simultaneously produce the proper carries for each of these stages. These carries are then applied to the adder block for each stage, which then produce the proper sum bit.

The conditional sum method requires that for each pair of bits to be added, two results are created. The first result, one sum and one carry bit per stage is prepared as the carry bit “0” entered the stage. The second result is prepared as though the carry bit “1” entered the stage. Next these results are examined in pairs. The second level result for a pair of stages is determined by the result of the first stage of the pair. This procedure is continued, examining the results in quartets, octets and so forth.

It is also possible to use a redundant signed-digit number system by which the carry propagation is drastically limited. In the conventional number system, there are B-symbols to denote the individual digits in a radix B in the redundant system the number of symbols used range from (B + 1) to (2B – 1). This redundancy is achieved by using a signed-digit format where each digit is signed. It has been shown by Avizienis (1961) that totally parallel additions are possible for certain redundancies. (See also Garner 1965) Schemes in which one of the operands is in conventional form and other in the signed-digit form have been found very useful. Atkins (1969 a, 1969 b), Robertson (1967 a), Rohatsch (1967), Borovec (1968). These limited carry propagation adders have been found to be very useful in designing fast adder-subtractor and multiplier.

**MULTIPLICATION SCHEMES**

We will discuss below some schemes which have been found to be very fast and convenient [Habibi and Wintz (1970)].

Let us assume that we have an n-bit multiplicand and an m-bit multiplier. Then we have n m partial products or summands to be summed up.

All these can be generated simultaneously by using n m NAND gates and complementing their outputs. Hence the basic problem in designing a high speed multiplier is to reduce the time required to add the summands.
4. DIVISION SCHEMES

The addition and multiplication operations are both associative, commutative and multiplication is distributive with respect to addition.

\[ a + b = b + a \]
\[ a \cdot b = b \cdot a \]
\[ (a + b) + c = a + (b + c) \]
\[ (a \cdot b) \cdot c = a \cdot (b \cdot c) \]
\[ a \cdot (b + c) = a \cdot b + a \cdot c \]

These properties help to simplify the algorithms used for high speed work by certain suitable segmentation of the operands.

The division problem is complicated by the fact that it does not satisfy these properties. Thus inherently some form of trial and error procedures are to be used for the division operation involving the division of multiple digit numbers. All the direct procedures for division necessarily involve the comparison of multiple digit numbers. The relative magnitudes of the divisor and the partial remainder at each stage of computing the quotient digit at each step is taken as the leading digit or the digit in every successive partial remainder and later adding a correction not exceeding unity. (Krishnamurthy 1970). This scheme requires an initial range transformation of the divisor and the dividend. The selection of the multiplier as a function of the leading digits of the divisor and a which involves the selection of a multiplier as a function of the selected digit is available. Since fast multipliers and very high speed read only memories are available, this scheme will be useful.

However, for every quotient digit the recursions involving a multiplication and subtraction are still needed; thus for each quotient digit one multiplication and one subtraction are necessary. The one disadvantage here is that the true remainder is not directly available.

The other possibility is to use segmented division schemes where one uses a truncated quotient and divisor and obtain a trial quotient. Under certain conditions the trial quotient can be corrected by simple logical tests to yield the true quotient digit. These division schemes belong to the class of divide and correct methods (Krishnamurthy 1965, 1967, 1970b, 1970c). Similar methods have been recently used in the III (Atkins 1968a, 1969b). The use of partial redundancy in division scheme is recently discussed (Krishnamurthy 1970).

An alternative is to use a sequence of simultaneous range transformations on the divisor and the dividend which cause the divisor to converge to unity and the dividend to quotient. These schemes which require an initial table look up and only multiplications, belong to the class of iterative schemes. (Essel Anderson, Earle, Goldschmidt and Powers 1967) and Krishnamurthy (1970a, 1970b, 1971). Further work in this direction has been carried out by Shaham (1970) and Flynn (1970).

These schemes need \( (1 + \log_2 \frac{a}{b}) \) multiplications for a bit quotient where \( n \) represents the number of leading unity digits or zero digits followed by a most significant unity digit in the initial division. Thus by a suitable choice of \( n \), involving a table look-up, high speed can be obtained. A division time comparable to the time required for multiplication seems to be attainable.

5. PHYSICAL BARRIERS IN SPEED-UP.

So far we were concerned with speeding up of the arithmetic operations. We shall now indicate that the speed of computers is almost reaching a limit that no further improvement in technology would be possible. This is due to the fact that physics sets up the barriers rather than technology. These barriers are beyond our control. We will discuss how these limitations arise and why we cannot overcome them; we would in addition point out the consequences.

a. The Light Barrier

We know that all the signals we use in computers are electrical pulses propagating at the speed of light. These signals cannot travel any faster. In one nanosecond (= 10^-9) light travels 30 cm = 1 foot. Thus if we use a random access memory which is used to oscillation of one cycle per foot.

b. Quantum Barrier

According to quantum mechanics electromagnetic oscillations are quantized and so other signals. With every moving particle there is associated which quantized such that the energy \( E \) of frequency \( v \) is associated can be observed, at least one quantum of signal is needed. This condition limits the frequency band that can be used for signalling to

\[
\frac{v}{c} \leq \frac{\hbar}{\hbar}
\]

where
- \( m \) = Mass of the system
- \( c \) = Velocity of light
- \( h \) = Planck's constant

Using Shannon's information theory it can be shown that the capacity (or rate of information) does not exceed \( mc^2/2h \) bits per second. The quantity \( h/c^2 \) is the mass equivalent of one quantum oscillation at one cycle per second.

Thus our proposition says: Information transmission is limited to frequencies such that the mass equivalent of a quantum of the employed frequency does not exceed the mass of the entire transmission or computing system. Each bit transmitted in one second requires a mass of at least

\[
\text{Mass of hydrogen atom} = 1.67 \times 10^{-27} \text{gm} \times 2 \times 10^{25} \text{gm} = 3.34 \times 10^{-2} \text{gm} \text{Sec}^{-1}
\]

Thus per mass of hydrogen atom no more than \( 2.3 \times 10^{22} \) bits/Sec can be transmitted.

The number of protons in the universe has been estimated to be around \( 10^{70} \). Thus if the time can be processed.

To a person unacquainted with the combinatorial problems this may seem to be large with practically no restriction at all. In fact, however, by the processes we hope to use in advanced computing, this limit only too quickly reached.

Example

Consider an artificial retina with million sensitive units, each of which can only be excited or not excited. It acts through a net that produces as output only a 1 bit move or not move. If we
ask "what is the relation between input and output?". This means there is a transformation of \(10^6\) possible input states to 2 output states.

The number of such mappings is \(2 \times 10^6 = 1\times10^{12}\) bits.

In the problem of chess we have \(10^{12}\) possible move sequences.

c. Thermal Efficiency and the Thermodynamical Barrier

Corresponding to information processing there is a change in the entropy of the system and hence there is some quantity of heat absorbed. This amounts to \(kT \log 2\) per bit where \(T\) is the absolute temperature, \(k\) is the Boltzmann's constant. It is not possible to economise any further on this.

It has been recently shown that certain micro-organisms like E coli produce information as they grow in a very efficient manner at \(kT \log e^{12}\) per bit.

For instance if we want to process \(10^{30}\) bits per second we need \(10^{30} \times 310 \times 7 \times 10^{-16}\)
\[\approx 3 \times 10^9\] watts.

\[k = 1.38 \times 10^{-16}\text{ erg/degree.}\]

d. Consequences

That nothing made of matter can transmit or process information faster than \(10^{47}\) bits per second per gram may seem of small practical importance. In fact many processes which aim for artificial intelligence in a machine require transmissions far in excess of this limit.

Not only our machines but the brain made of matter is also thereby restricted.

Also the limit of about \(10^{102}\) bits/year implies that we can never study fully the relation between more than about 350 binary variables \(2^{350} \approx 10^{102}\) and hence we cannot study the general relation when intrinsic complexity exceeds 300.

REFERENCES


27. Robertson, J.E., 1967 b, "The Correspondence between methods of digital division and multiplier recording procedures", Report No. 252, Department of Computer Science, University of Illinois, Urbana.


CHAPTER NEWS

Eastern India Chapter

ELECTION OF NEW MEMBERS TO THE MANAGING COMMITTEE

Mr. P. P. Uttamsingh of Union Carbide (India) Ltd. and Mr. M. S. V. Rao of Indian Statistical Institute were unanimously elected to the Managing Committee in places of Mr. S. S. Rangarajan and Mr. S. Ganesan, in the annual general body meeting held on 18 December 1970.

OFFICE BEARERS FOR 1970-71

Chairman: Mr. P. P. Uttamsingh
Secretary: Dr. J. Roy
Treasurer: Mr. M. S. V. Rao
Members: Mr. R. M. Bhandari, Mr. N. D. Deo and Dr. B. Nag

CURRENT STRENGTH

There are at present 10 institutional members and about 57 individual members in the chapter.

MEETINGS

Prof. R. A. Buckingham, Director of the Institute of Computer Science in the University of the British Computer Society and Computer Education in U.K.

London met the members of the chapter on 19 February 1971 and gave an account of the activities of the chapter was held at Bhilai Steel Plant on 17 April, 1971.

Delhi Chapter

FORMATION

The question of forming the Delhi Chapter was first raised at the conference of the Computer Society of India held at Trivandrum in December 1968. It was left for members from Delhi to take an initiative. Consequently, Computer Society of India members from Delhi proposed to form the Delhi Chapter of the Computer Society of India at a meeting held at Indian Institute of Technology, Delhi.
VISITS TO COMPUTER CENTRES

The Delhi Chapter arranged the following visits to different Computer Centres of Delhi during the period 1973-74:

1. Computer Centre of the Textile Division, Delhi Cloth Mills on 12-11-74;
2. Computer Centre of the Department of Statistics, Government of India, R.K. Puram on 22-4-74;

The visits were preceded by explanatory talks by the personnel of the respective Computer Centres. The Chapter is grateful to the authorities of these centres for extending their cooperation.

PROFESSIONAL TALKS

The following professional talks were arranged by the Chapter:

1. On 8th January 1974, a talk by Shri N. S. Josan, Student Member of the Chapter, was arranged in the TNO Auditorium. The subject matter of the talk was "A Typical Industrial Simulation". Shri Josan covered the various aspects of simulation of physical problems on digital computers and gave details of a specific industrial simulation with relation to textile mill.
2. On 22nd February 1974, a talk by Shri A.S. Raihead, Secretary, Delhi Chapter, was arranged in the TNO Auditorium. The talk was on "Computational Information Networks in USA". The talk highlighted computerised information networks via a via the role of scientists and technical information. The presentation term information networks was illustrated from the discipline of physics application.

The Chapter is grateful to the authorities of TNO for making their auditorium available for these talks.

SEMINARS

It was decided by the Executive Committee, at its meeting of 12-10-70, to hold a Seminar in March 1971 to create popular awareness of the impact of computing in a developing country like India as well as on the progress made in computer hardware and software along with the Computer Society of India Conference. The Seminar had to be postponed in view of the decision of the Computer Society of India to hold its next Conference at Bombay.

PROFESSIONAL ADVANCEMENT COURSES

The following sub-committee was constituted to draw-up the programme for Professional Advancement Courses:

1. Shri N. C. Khandekar
2. Shri A.S. Raihead
3. Shri K.D. Sharma

The first course in this series will be "FUNDAMENTALS OF COMPUTER SCIENCE" to be followed by a course on Information Retrieval etc. The members can look forward for the announcement.

CONSULTANCY SERVICE

The proposal for setting up a Consultancy Service by the Chapter was discussed and approved by the Executive Committee at its meeting held on 12-2-71. A sub-committee of Shri S.K. Saha

Gupta, Shri A. S. Raihead and Dr. K.D. Sharma was constituted to work out the details of this service. The report of the Sub-Committee is awaited.

CLIP SERVICE

The Pilot Fascicles of the CLIP Service—Computer Literature on Information Processing—was issued by the Chapter and comments from the members are being invited. It is hoped that the members to whom the copies of the CLIP service were sent will send the questionnaires.

It is proposed that the CLIP Service will include the review articles of interest. The Service is likely to be made available to the members free of cost with the financial assistance from the Computer Society of India. The details are in preparation.

Finally I would like to thank all the members for their active participation in the activities of the Chapter. I wish to thank the members of the Executive Committee for their excellent cooperation, without which it would not have been possible to do even this much in such a short time.

Bombay Chapter News

Chairman:
Shri P.C. Kohli

Secretary:
Shri S.S. Thakur

Treasurer:
Shri G.S. Sankaran

Tata Consultancy Services
Bombay Suburban Electric
Nirmal, Nariman P.
Bombay-1

Supply Ltd.
Agra Road, Bombay-70.

Eclectic House,
SantaCruz East, Bombay-55 AS.

EXECUTIVE COMMITTEE MEMBERS

Dr. P.V.S. Rao (TEPR)

Shri S.S. Shrikhande (Philips India)

Shri P. Jayant (Air-India)

ADDRESS FOR CORRESPONDENCE

Shri Sarwottam S. Thakur
Bombay Suburban Electric Supply Ltd.
SantaCruz East, Bombay-55 AS.

The present membership consists of 20 institutions and 30 individuals.

During the recent months, the Chapter organized three talks: 'Audio Tapes for Computer Input', by Dr. H.V. Sahasrabuddhe of IIT-Kanpur and 'Recent Development in Industrial Logic and Drive Controls' by Mr. V.N. Dravid were two of these. There was also a lecture on 'The Computer Languages' by Dr. Mathakuran. The first two of these talks were held in cooperation with IIT, IITM and IITB.

Most of the members of the Bombay Chapter who are users of IBM equipment were quite concerned about the recent announcement by IBM of an increase in the monthly rental and maintenance
charged. Meetings were held to discuss these and the Chapter arranged a meeting with Mr. A. L. Taylor, IBM’s General Manager, to express its views on the subject of the maintenance and rent increase, and to hear IBM’s side.

The next annual Conference is scheduled to be held on the 26th, 30th and 31st December 1971 in Bombay. National Institute for Training in Industrial Engineering (NTIE for short) which is situated on a hillock overlooking the Viceroy and Poval lakes has been chosen as the venue for the meeting.

Ahmedabad Chapter,

OFFICE BEARERS FOR 1971

Shri S. R. Thakore
Shri B. D. Srinivasan
Shri Y. Shenivasan
Shri K. J. Shroff
Shri K. Rajagopal
Prof J. G. Krishnaya

Chairman
Secretary
Treasurer
Managing Committee Members

CURRENT STRENGTH:

Institutional Members 5 (from one Institution)
Individual Members 58
Total Members 63

CHAPTER ACTIVITIES:

April 27, 1971 — Shri K. M. Narayanan, Sr. Programmer of TELER, Trivandrum delivered a lecture on “Fortran Compiler for Minak-2 Computer.” This was attended with.

June 29, 1971 — A Seminar was held by the Chapter on ‘Operations Research’. Shri T. S. Anand, of IBM New Delhi participated and presented a paper on “The Computers and Operations Research” with specific reference to corporate planning. A large number of members of the Ahmedabad Branch participated in this Seminar.

OTHER ITEMS

A letter regarding “IBM Machine Rental Increase” was written to the President of the CSI, requesting him to take necessary action with the IBM as well as the Government of India. Copy of

SEVENTH ANNUAL CONFERENCE

Preparations for the Seventh Annual Conference are well underway. The steering committee consisting of Dr. P. V. S. Rao (TIFB), O. C. Kohli (TOS), Mr. P. Jayant (Air India) and Mr. T. V. Balan (ACC), is sparing no pains to organise the conference with utmost care and meticulousness. It is a safe prediction that participants will have a very pleasant, useful and rewarding time in Bombay during 26th through 31st December 1971.

The first Brochure on the conference has been printed and mailed to all members by the Steering Committee.

CSI JOURNAL

The second issue of the journal will be despatched to subscribers by the first week of September 1971 at the latest.

ELECTRONICS CORPORATION OF INDIA

Electronics Corporation of India Ltd (ECIL) has recently submitted a project for making electronic central processors for small and medium-sized computers in the country. With indigenous know-how and existing equipment needed for this project, the complete computer systems will have to be imported at present. The Electronics Commission has approved this proposal and is allocating finances for the developmental activity envisaged in this proposal.

MEMBERSHIP SUBSCRIPTION

Members who have not paid their subscription for the current financial year, 1971-72, are requested to send in their subscription to the Secretary.

UPDATED LIST OF ADDRESS

Institution Members:

All Institution members have been addressed requesting an updated list of nominees from the respective institutions.

Institution Members:

This Newsletter is being posted to members at the addresses we have on record. Members are requested to intimate the secretary about the change of correction to addresses if any.
<table>
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<tr>
<th>S. No.</th>
<th>Name of the Institution</th>
<th>System</th>
<th>Members</th>
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| 104   | Larsen & Toubro Ltd      | IBM 1401 | Dr. Shyam Kumar  
|       | Powai Works              |        | Shri Y. A. Sapre   
|       | Saki-Vihar Road,         |        | Shri L. D. Parulekar 
|       | Bombay-72 AS             |        | Shri P. S. Rao     
|       |                          |        | Shri S. G Ravikumar|
| 105   | India Meteorological Dept.| IBM system/360 Model 44F | Shri K. N. Rao  
|       | Lodi Road, New Delhi-3   | Philips Model DS 714 | Dr. P. K. Das    
|       |                          |        | Shri S. K. Das     
|       |                          |        | Shri D. Krishna Rao|
|       |                          |        | Shri S. B. Kulkarni|
| 106   | Institute of Defence Management |        | Brig V. Dhrula  
|       | Secunderabad-15          |        | Capt. S. S. Rao   
|       |                          |        | Gp. Capt. Satinder Singh |
|       |                          |        | Wg-Cdr. M. K. Challu |
|       |                          |        | Lt. Col. Kannamatta Singh |
| 107   | Business Forms Limited   |        | Shri Baldev Sud   
|       | 6-A, Middleton Street,   |        | Shri S. P. Ahuja   
|       | Calcutta-16              |        | Shri B. N. Arora   
|       |                          |        | Shri R. K. Sood    
|       |                          |        | Shri H. K. Chawla  |
| 108   | Instrument Research and Dev. Estt. |        | Prof. G. Mukharji |
|       | Ministry of Defence      |        | Prof. R. C. Goyal |
|       | Dehra Dun                |        | Dr. V. Gupta      
|       |                          |        | Shri Merecha J. K. Gupta |
|       |                          |        | Shri Jagdish C. Kapur |
| 109   | The Indian Institute of Public Administration, Indraprastha Estate |        | Prof. G. Mukharji |
|       | Ring Road,               |        | Prof. R. C. Goyal |
|       | New Delhi-1              |        | Dr. V. Gupta      
|       |                          |        | Shri Merecha J. K. Gupta |
|       |                          |        | Shri Jagdish C. Kapur |
|       |                          |        | Shri G. S. Shah    
|       |                          |        | Shri K. S. Krishnan|
|       |                          |        | Shri K. J. Patel   
|       |                          |        | Shri J. V. R. Adusumalli |